ABSTRACT

Methods of forming MOSFET devices featuring LDD regions offset from the edges of conductive gate structures has been developed. A first embodiment of this invention features the definition of a tapered conductive gate structure with the foot of the tapered structure larger in width than the top of the structure. Formation of an LDD region is accomplished in regions of the semiconductor substrate not covered by the tapered conductive structure. A dry etch procedure is next used to remove the foot of the tapered conductive structure resulting in an LDD region being offset from the edges of a now straight walled conductive structure. A second embodiment of this invention entails the definition of a conductive gate structure featuring notches located at the bottom of the conductive gate structure, extending inwards. Formation of an LDD region is again accomplished in regions of the semiconductor substrate not underlying the non-notched portion of the conductive gate structure, resulting in the LDD region being offset from the notched edges of the conductive gate structure.